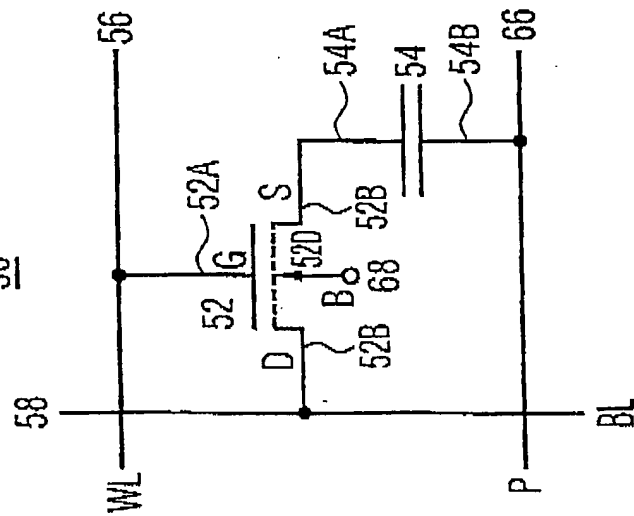


FIG 4A
(PRIOR ART)
50

(PRIOR ART)

51


$$w_L = \text{word line}$$

BL = bit line

P = common capacitor plate

FIG 4B

(PRIOR ART)

50

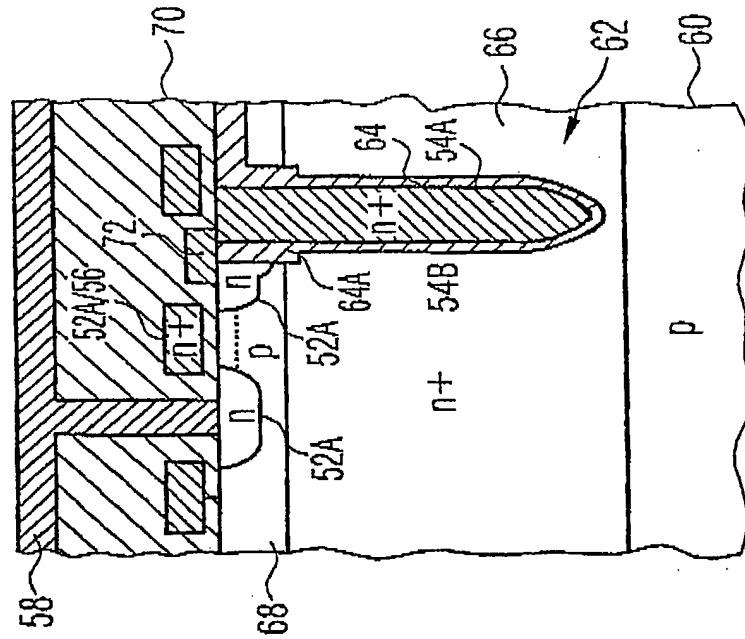


FIG 5A
(PRIOR ART)

vertical MOSFET

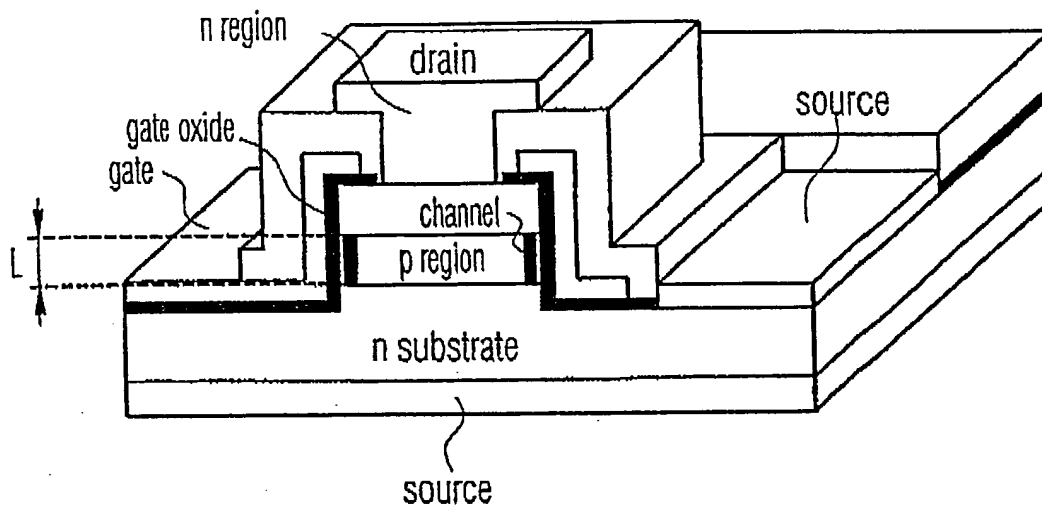


FIG 5B
(PRIOR ART)

